EGC442
Class Notes
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Baback Izadi
Division of Engineering Programs
bai@engr.newpaltz.edu

•**Required design documentation for the Project**

1. Register file: With appropriate detail, show the layout of the register file.

2. ALU: You need to show a detailed design of an ALU to support the following instructions:

Table 4: Instruction set for required design

1. Data Path: Show the data path of each class of instruction as well as the overall data path per Table 4.

a. Control: Develop the control logic to support your instructions. Gate level design in not necessary. However, functional table needs be very detailed and clear, making it implementable in an FPGA.

2. Pipelined Data Path: Show the data path for the pipelined architecture.

Extra Credits (20 Points):

Note: Extra Points are only considered if the processor design is over 80% correct.

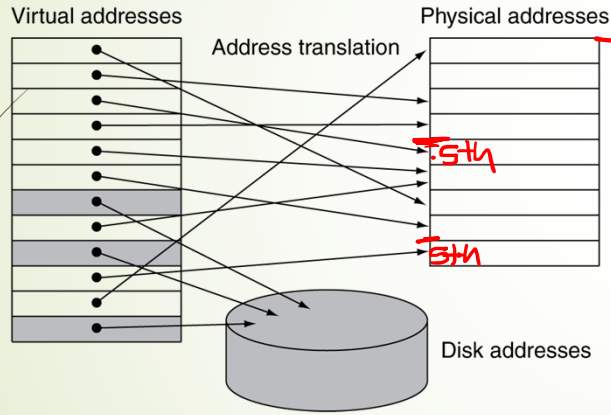
Either Verilog code or a schematic capture of the ALU is needed. Documentation should include two simulation cases for each ALU operation.

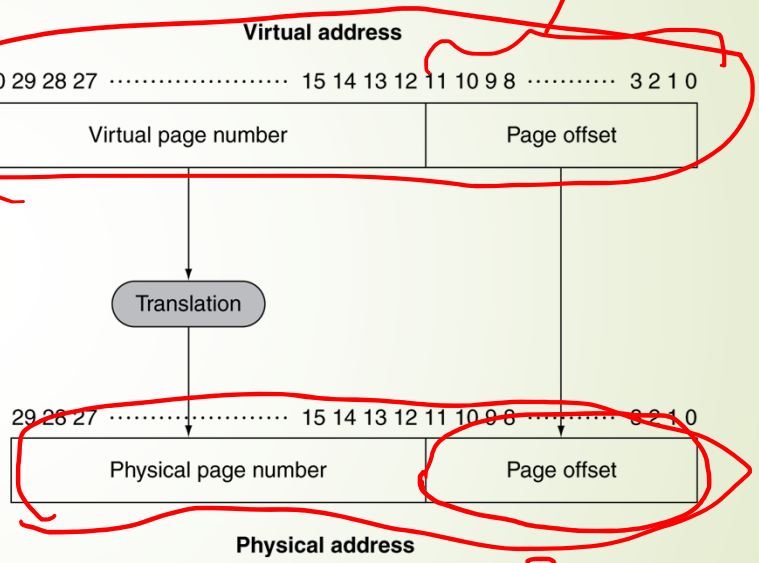
	Score	/Max Point
Register File	9	/10
ALU Design	13	/15
Data Path	27	/30
Control	15	/15
Pipelined Data Path	14	/15
English	14	/15
TurnItIn similarity negative score	0	
Total	92	/100
Extra Credits		/20
Total Course Project	92	/100
Applicability for Design Folder:		
	X	Yes
		No

Instruction	Operation	ALU function
LDUR	load register	add
STUR	store register	add
CBZ	Conditional branch on zero	pass input b
CBNZ	Conditional branch on not zero	pass input b
B	Unconditional branch	
R-type	add	add
	subtract	subtract
	AND	AND
	ORR	OR

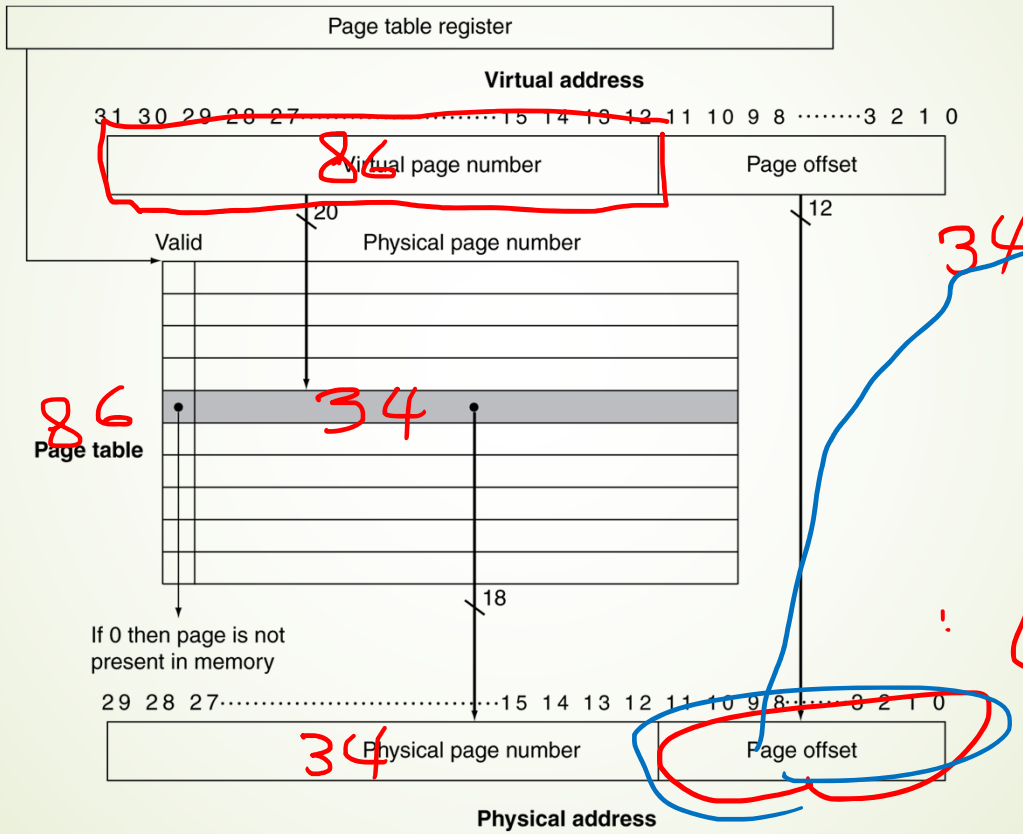
Address Translation

- Fixed-size pages (e.g., 4K)

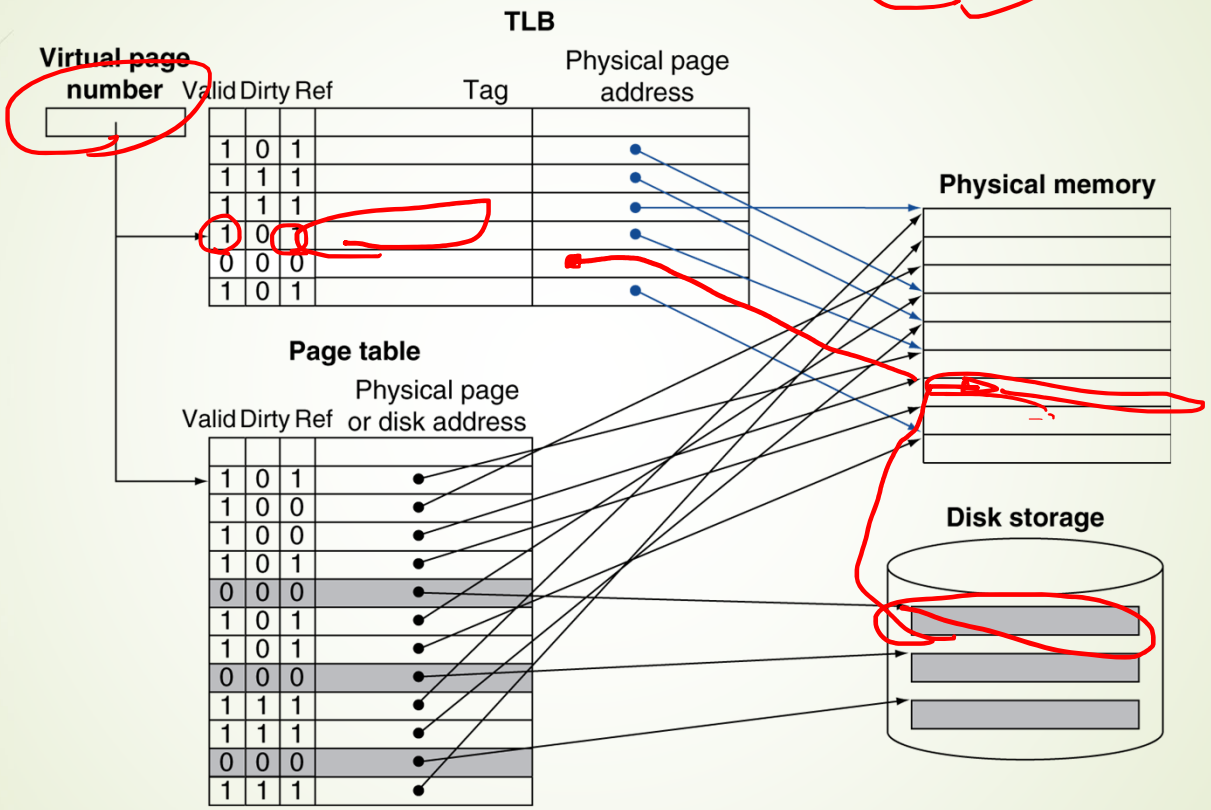




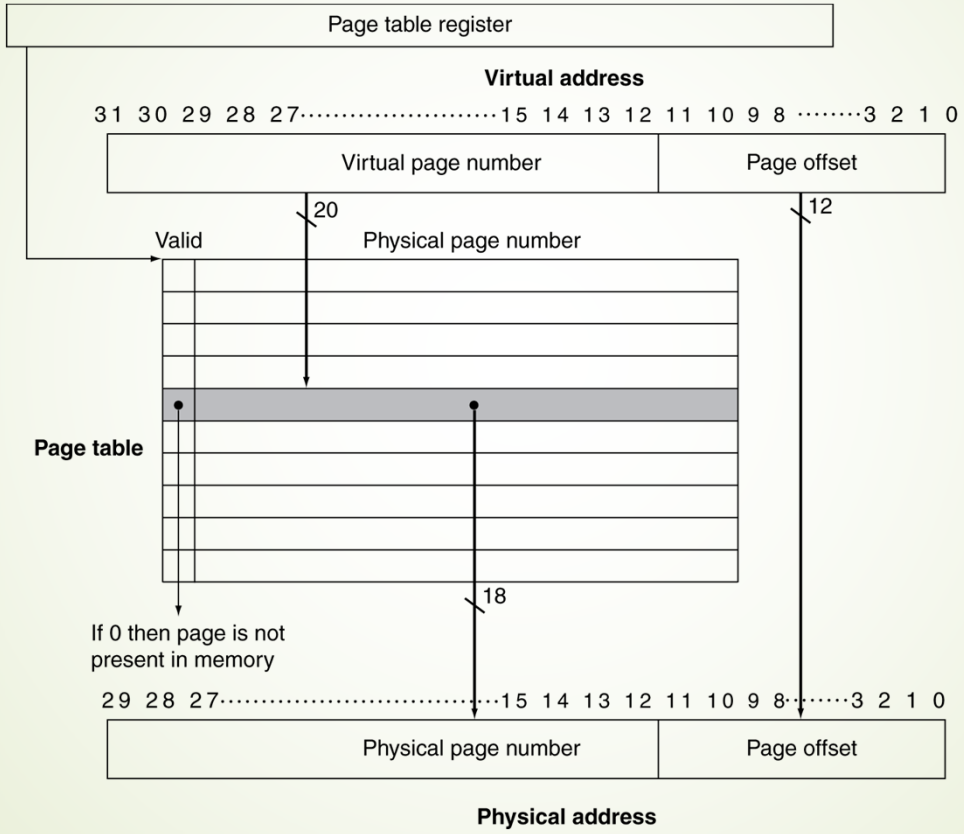
Translation Using a Page Table



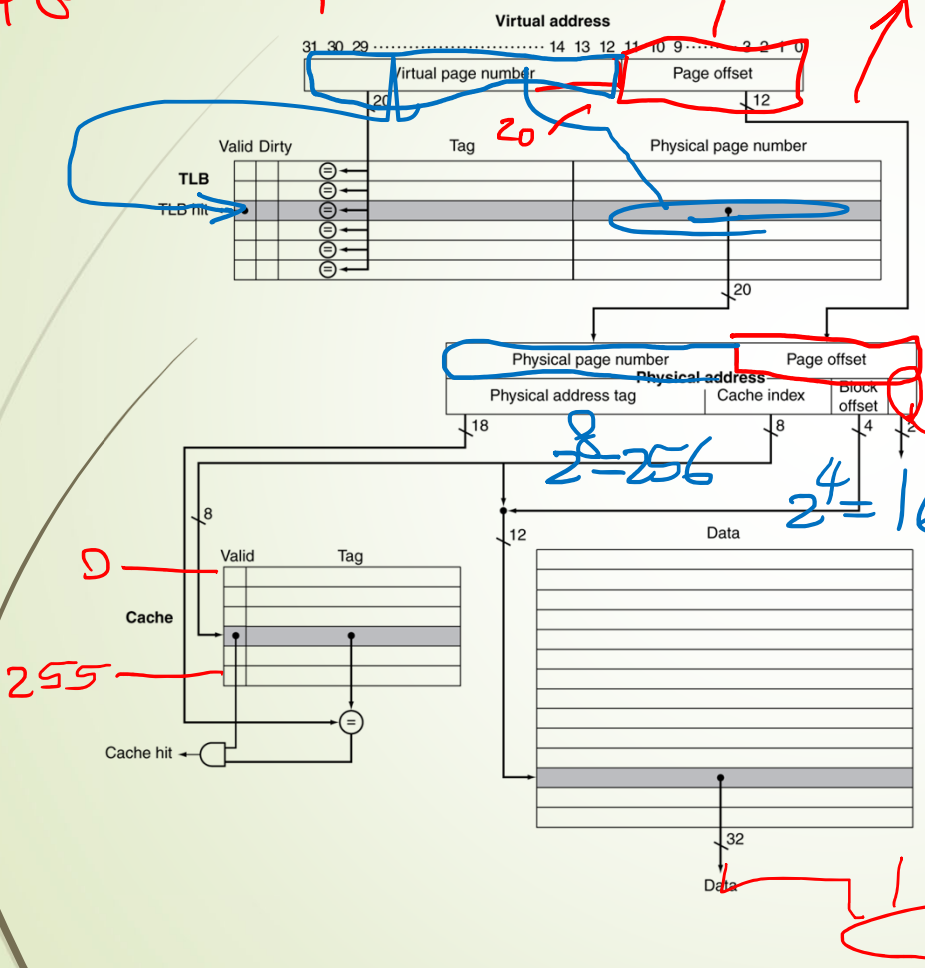
Fast Translation Using a TLB



Translation Using a Page Table



TLB and Cache Interaction



- If cache tag uses physical address
  - Need to translate before cache lookup
- Alternative: use virtual address tag
  - Complications due to aliasing
  - Different virtual addresses for shared physical address

1) A virtual machine (VM) is an emulation that provides a hardware interface.

- ○ True
- ◉ False

Correct

A virtual machine is an emulation that provides a *software* interface.

2) A system VM allows a computer to share hardware resources amongst multiple operating systems.

- ◉ True
- ○ False

Correct

If a computer is running copies of many different operating systems (OSes) using VMs, each OS needs to use the hardware resources.

3) When a computer runs multiple VMs, the first VM launched is called the host, and the other VMs are called the guests.

- ○ True
- ◉ False

Correct

The computer hardware running the VMs is the host, and the VMs are the guests.

4) Another name for a VMM is a hypervisor.

- ◉ True
- ○ False

Correct

The VMM (virtual machine monitor) or hypervisor is the software the supports virtual machines. The VMM determines how to map the VMs' virtual resources to physical hardware resources.

5) A VMM is the same size as the corresponding OS.

- ○ True
- ◉ False

Correct

The VMM is a reduced version of a full OS.

6) A VMM should not allow a guest VM to change how resources are allocated.

- ◉ True
- ○ False

Correct

A VMM should also run a guest VM as if the VM is on the native hardware.

7) A VMM runs in system mode, while a guest VM runs in user mode.

- ◉ True
- ○ False

Correct

The VMM must have a higher privilege level than a guest VM. System mode provides a more privileged set of instructions that can be used to control all system resources.

3

Protection	Mechanisms that prevent multiple processes that use the same hardware from interfering with each other. One such mechanism is the translation of a program's address space to a physical address accessible only to this program.	Correct
Virtual memory	A technique where main memory is used as a cache for secondary storage. Virtual memory is used to safely share memory amongst programs and remove the burdens related to the limited size of main memory.	Correct
Address mapping	The process of mapping a virtual address to a physical address. Address mapping is also called address translation. The physical address may map to a location in main memory or disk.	Correct
Virtual address	An address that corresponds to a location in virtual space. Address mapping assigns a virtual address to a physical address when memory is accessed. Multiple virtual addresses can be mapped to a single physical address.	Correct
Page fault	A virtual memory miss. A page fault occurs when an accessed page is not in main memory.	Correct

9 In a virtual memory system, an ____ is typically written to the disk.

- ○ individual word
- ◉ entire page

Correct

Writes can take millions of processor clock cycles, so copying back an entire page is more efficient than writing individual words back to the disk.

10 A ____ bit indicates if a page has been written since being read into memory.

- ◉ dirty
- ○ use

Correct

A dirty bit is set when any word in a page is written and indicates if a page needs to be copied back when the page is replaced. Alternatively, a reference bit or use bit is set when a page is accessed, regardless of whether the page is written to, to indicate if the page was touched during a particular time period and is a good candidate for replacement.

11

cache	The TLB, or translation-lookaside buffer, is a special ____ that keeps track of recently used translations. The TLB allows the processor to avoid accessing the page table, which is located in memory.	**Correct**
status bits	Each TLB entry includes the physical page address, tag, and ____ . The TLB, rather than the page table, is accessed for every reference. Thus, the TLB must similarly include a valid, reference, and dirty bit.	**Correct**
fewer	A TLB has ____ number of entries as a page table. A TLB has many fewer entries than a page table, relying on locality of reference to improve access performance.	**Correct**
write-back	A TLB entry is replaced using a ____ scheme. Only the reference and dirty bits need to be copied back to the page table entry when the TLB entry is replaced, as these bits are the only portion of the TLB entry that can be changed.	**Correct**

Are the following TLB, virtual memory system, and cache miss combinations possible or impossible?

a) TLB hit, page table miss, cache miss

- Possible
- Impossible

Correct

A TLB translation cannot occur if the page is not in memory.

b) TLB miss, page table miss, cache hit

- Possible
- Impossible

Correct

Data cannot exist in a cache if the page is not in memory.

c) TLB hit, page table hit, cache miss

- Possible
- Impossible

Correct

Though possible, the page table will not be checked if there is a TLB hit.

d) TLB hit, page table miss, cache hit

- Possible
- Impossible

Correct

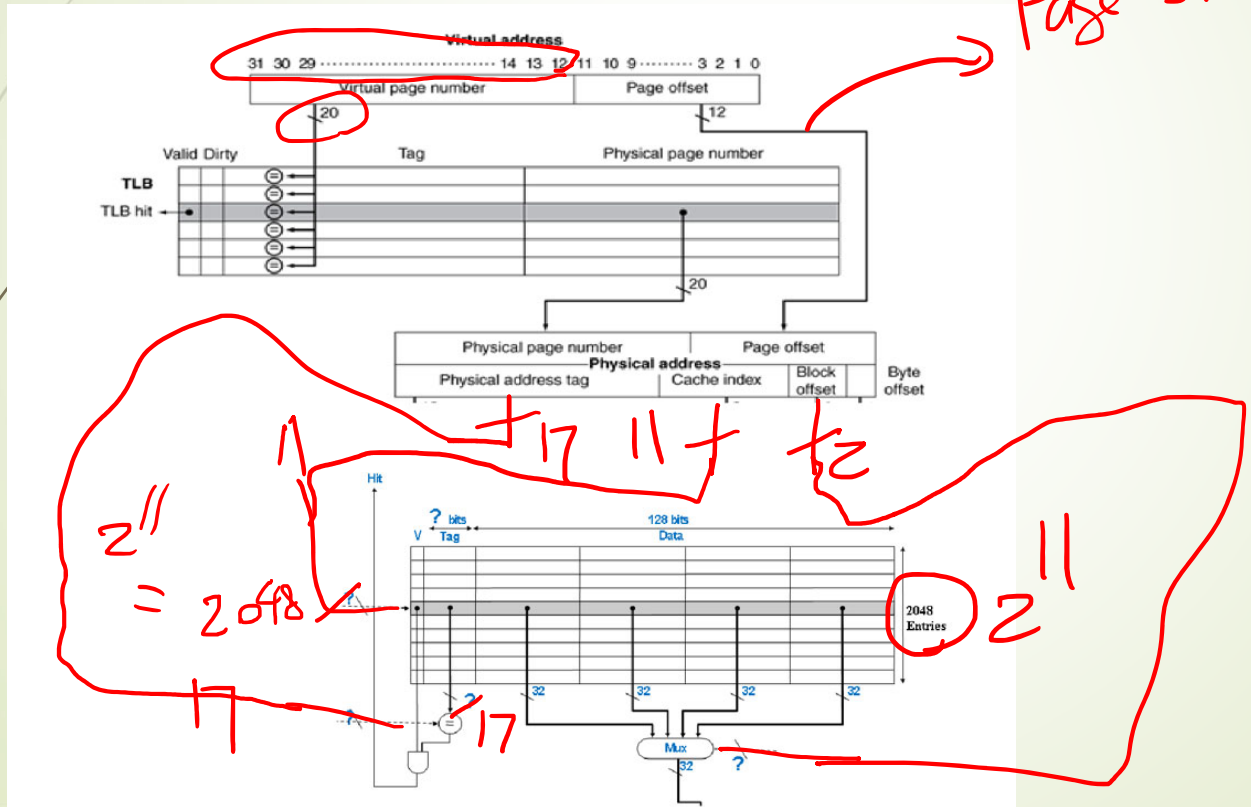
A TLB translation cannot occur if the page is not in memory.

L1 cache	A cache for a cache. L1 cache, known as the primary cache, can be used as a cache for the L2 cache if the L2 exists.	**Correct**
L2 cache	A cache for main memory. The L2 cache is faster than main memory, but tends to be larger and slower than the L1 cache.	**Correct**
Main memory	A cache for disks. The virtual memory technique uses main memory as a cache for data on disks.	**Correct**
TLB	A cache for page table entries. The translation look-aside buffer stores recent address mappings to avoid page table accesses.	**Correct**

14) The figure below depicts the memory system.

a. What is the function of TLB? cache for page table
b. How many virtual pages numbers does the system have and how many bytes is each page? $2^{20} = 1M$
c. Identify type of cache architecture direct mapped block size 4 words
d. Complete the cache architecture by connecting the dash lines to appropriate physical address. Identify how many bits is each connection.

Page size = 2^{12} = 4K



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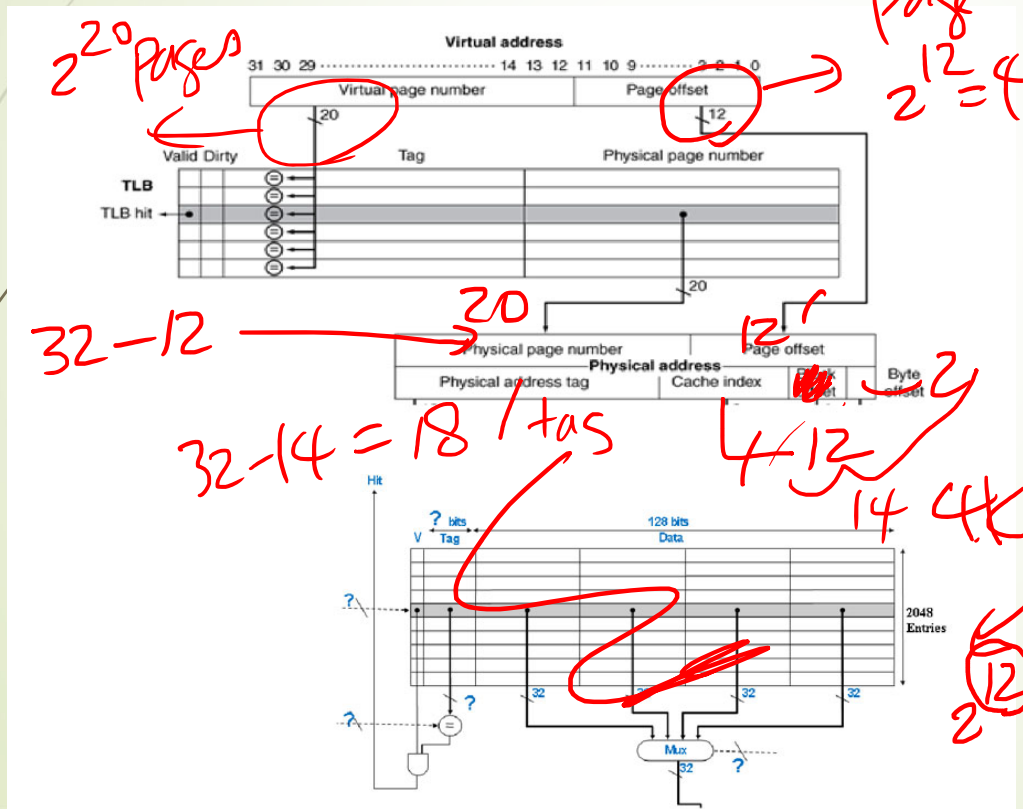

14) The figure below depicts the memory system.

a. Modify it for 4 way associative cache.